

REMARKS

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (Japanese Patent Publication 01-107527) in view of Adair (US Patent 6,184,151). Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Patent 6,492,073) in view of Adair.

1. Objection of the specification:

The objection of Paper No.4 to the abstract of the disclosure because it had more than 150 words is now withdrawn because a new amended abstract of acceptable length has been received in Paper No.5. However, the amended abstract is still objected to since it has not been submitted on a separate sheet, as requested in the previous Office action (Paper No.4).

Response:

The amended abstract of the disclosure has been re-submitted on a separate sheet as requested in the Office action. In order to correspond with the amended claim 1, the phrase "cutting the plurality of lines of the first exposure regions" is changed to "that are rectangles interlaced with and perpendicular to each other on the photoresist layer and do not overlap the first exposure regions". In order to shorten the abstract of the disclosure to less than 150 words, the term "The array photoresist layer" is deleted. Reconsideration of the corrected specification is politely requested.

30 2. Rejection of claim 1 under 35 U.S.C. 112:

Claims 1 (as amended) is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The "cutting the plurality of lines of the 5 first exposure regions" at page 8, line 32 to page 9, line 1 of the amendment (Paper No.5) does not find basis in the original disclosure. It is also not clear whether the "cutting" of the first exposure regions with subsequent exposure regions involves double exposure (overexposure) or not. Therefore, 10 this new phrase is considered new matter and is not enabled by the specification.

Claim 1 (amended) is rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which 15 applicant(s) regard as their invention. Evidence that claim 1 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in Paper No.5, filed 30 January 2003. In that paper, applicant has stated at page 6, lines 30-31 that "no overexposure areas are formed due to twice 20 exposure", and this statement indicates that the invention is different from what is defined in the claim(s) because the "cutting" of claim 1 reads on crossing or overlapping exposure areas (overexposure areas).

25 **Response:**

Claim 1 has been amended for overcoming the rejection of 35 U.S.C. 112. The term "cutting the plurality of lines of the first exposure regions" is changed to "that are rectangles interlaced with and perpendicular to each 30 other on the photoresist layer, and the second exposure regions doing not overlap the first exposure regions". The amended portion is disclosed in the specification from

page 9, line 15 to page 10, line 1, Fig.11, and Fig.12. No new matter is included. Reconsideration of the currently amended claim 1 is politely requested.

5 **3. Rejection of claims 1-2 under 35 U.S.C. 103(a):**

Ueno teaches a method of preventing two-dimensional (optical proximity) effects caused by light diffraction during a photolithography process to form (define) a rectangular (array) pattern. A negative photosensitive resin 10 (photoresist) is formed on a semiconductor substrate. The photoresist is exposed through a first linear mask pattern, 100 (having parallel lines, 101), shown in Figure 1(a). Then 15 the photoresist is exposed through a second linear mask pattern, 200 (having parallel lines, 201), shown in Figure 1(b) and positioned in perpendicular relation to the first exposure pattern to form an array of rectangular unexposed photoresist regions, 400, shown in Figure 2(a).

Ueno does not specify subsequent etching of the substrate using the remaining photoresist pattern as an etching mask 20 and does not specify the formation of storage nodes for a dynamic random access memory (DRAM). Ueno also does not specify that the optical proximity effects to be avoided were corner rounding and pattern shortening.

Adair states that in order to scale down DRAM devices while 25 maintaining sufficient capacitance, corner rounding and shortening effects should be avoided when forming the storage nodes (capacitors) in column 1, at lines 46-53. Adair also teaches plural perpendicular exposures (using masks having parallel linear patterns) of one or more photoresist layers 30 to obtain sharp-edged corners (without significant corner rounding or image shortening) in the resulting photoresist image, followed by etching of an underlying substrate through

the remaining photoresist pattern as an etching mask in column 6, at lines 6-50.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the Ueno 5 double exposure method to form a rectangular array of unexposed photoresist portions with the DRAM storage node formation by subsequent etching taught by Adair. The expected result of this combination would be to avoid corner rounding and image shortening during DRAM storage node formation.

10

Response:

First, claim 1 is amended in the above AMENDMENTS TO THE CLAIMS section to overcome this rejection and the newly added portion is disclosed in the 15 specification from page 9, line 15 to page 10, line 1, Fig.11, and Fig.12. No new matter is introduced.

Second, the Applicant intends to point out the difference between the amended claim 1 of the present 20 application and the combination of Ueno's and Adair's disclosures. The amended claim 1 of the present application is repeated below:

1. (Currently Amended) A method of forming storage nodes in a 25 dynamic random access memory (DRAM) on a semiconductor wafer, the semiconductor wafer comprising a substrate, a thin film layer positioned on the substrate, and a photoresist layer positioned on the thin film layer, the method comprising:

30 performing a first exposure process to form **first exposure regions that are lines parallel with each other on the photoresist layer;**

performing a second exposure process to form **second exposure**

regions that are rectangles interlaced with and perpendicular to each other on the photoresist layer, and the second exposure regions doing not overlap the first exposure regions;

5 performing a development process on the first exposure regions and the second exposure regions of the photoresist layer;

removing the first exposure regions and the second exposure regions of the photoresist layer to form an array photoresist layer on the thin film layer; and

10 using the array photoresist layer as a mask to perform an etching process to remove portions of the thin film layer not covered by the array photoresist layer so as to form an array thin film layer, the array thin film layer being used as the storage nodes in the DRAM.

15 In the present application, a method of forming storage nodes in a DRAM on a semiconductor wafer is provided. The method comprises performing a first exposure process to form first exposure regions that are lines parallel with each other on the photoresist layer, and performing a second exposure process to form second exposure regions that are rectangles interlaced with and perpendicular to each other on the photoresist layer, and the second exposure regions do not overlap the first exposure regions. The first exposure regions and the second exposure regions of the photoresist layer are 20 then removed to form an array photoresist layer on a thin film layer positioned on the semiconductor wafer. The array photoresist layer functions as a mask to perform an etching process to the thin film layer for forming an array thin film layer as storage nodes in the DRAM. Since the second exposure 25 regions do not overlap the first exposure regions, there is no overexposure area formed by the double exposure processes 30 according to the present application.

Ueno (Japanese Patent Publication 01-107527) provides a method for forming patterns and eliminating two-dimensional effect due to the diffracting of a light. As shown in the 5 figures, the method uses two photo masks for forming rectangular patterns, and each of the rectangular pattern is defined by each crossing part of the linear mask patterns of the two photo masks.

10 Adair (US 6,184,151) provides a method for forming images having sharp corners during lithographic processing and a photomask formed thereby. As shown in Fig.4 to Fig.7, a blocking layer 120, a hard mask 130, and a photoresist layer 140 are formed on a substrate 112 in sequence. Then a defining 15 process is performed to **form a plurality of parallel lines in the hard mask 130**. Another photoresist layer 150 is thereafter formed on the substrate 112. After that, another defining process is performed to **form a plurality of line patterns perpendicular to the lines of the hard mask 130 in** 20 **the blocking layer 120**. As a result, portions of the substrate 112 is exposed.

Both of Ueno's invention and Adair's invention disclose a double exposure method to form a rectangular array 25 corresponding to unexposed photoresist portions. Since the rectangular pattern is defined by each crossing part of the linear mask patterns of the two photo masks by double exposure process, overexposure phenomenon is inevitable to result in corner rounding problem. That means, portions of the 30 photoresist layer are exposed twice to form a plurality of overexposure areas, and the overexposure causes more severe optical proximity effects. **Because the size of the rectangular**

patterns are smaller than that of the d sign, the size of the subsequently formed storage nodes are also smaller than the design size. The combination of Ueno's invention and Adair's invention never teaches how to avoid the overexposure problem,
5 which is taught in the present application.

Furthermore, both of the first exposure processes and the second exposure processes in Ueno's invention and Adair's invention utilize a photo mask having parallel linear patterns
10 to form first exposure regions and second exposure regions, and the overlap between the first exposure regions and the second exposure regions forms a plurality of overexposure areas. Oppositely, the first exposure process and the second exposure process in the present application method utilizes
15 a photo mask having parallel linear patterns and a photo mask having rectangle patterns interlaced with and perpendicular to each other respectively to form first exposure regions and second exposure regions not overlapping the first exposure regions. With the pattern designs of the photo masks in both Ueno's invention
20 and Adair's invention, the same result can never be achieved.

From the above discussion, the Applicant believes that the amended claim 1 of the present application is absolutely different from the combination of Ueno's
25 invention and Adair's invention. Reconsideration of the rejection over the amended claim 1 is hereby requested.

As claims 2 is dependent upon the amended claim 1, it should be allowed if the amended claim 1 is allowed.
30 Reconsideration of the rejection over claim 2 is therefore requested.

4. Rejection of claims 1-2 under 35 U.S.C. 103(a):

Lin teaches a process of microlithography (photolithography) to avoid line end shortening caused by optical proximity effects. Column 6, lines 51-65 describes 5 first exposure of a photoresist through transparent parallel line segments 600 of a first photomask shown in Figure 18A to form corresponding latent image line segments in the photoresist, then second exposure of end portions of the image line segments in the photoresist with a cutting mask having 10 cutting elements 610 shown in Figure 18B. Lin also states that the order of these exposure steps can be reversed and that these masks and steps can be used equally well for forming images in either positive or negative resists. It should be clear that such cutting of the line segments would also remove 15 other defects at the line ends, such as corner rounding.

Lin does not specify subsequent etching of the substrate using the remaining photoresist pattern as an etching mask and does not specify the formation of storage nodes for a dynamic random access memory (DRAM).

20 It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the Lin photolithography method involving a first exposure and second cutting exposure to form a rectangular array of unexposed photoresist portions with the DRAM storage node formation by 25 subsequent etching taught by Adair. The expected result of this combination would be to avoid corner rounding and image shortening during DRAM storage node formation.

Response:

30 The present application provides a method of forming storage nodes in a DRAM on a semiconductor wafer. The method comprises performing a first exposure process to form first

exposure regions that are lines parallel with each other on the photoresist layer, and performing a second exposure process to form second exposure regions that are rectangles interlaced with and perpendicular to each other on the photoresist layer, and the second exposure regions do not overlap the first exposure regions.

Lin (US Patent 6,492,073) provides a mask set of two masks and a method of utilizing these masks in a double exposure process to avoid line shortening due to optical proximity effects. As shown in the figures, a pattern having pattern elements comprising a number of line segments, wherein each of the line segments has one or two free ends which are not connected to other mask pattern elements is to be transferred to a layer of resist. A first mask having transparent regions corresponding to the pattern is formed. A second mask (cutting mask) having transparent regions corresponding to the cutting pattern is formed. The cutting pattern comprises rectangles having the same widths as the line segments, and length to each of the free ends of the line segments.

By utilizing the principle of underexposure, there is no need for the present application to utilize a cutting mask to form the storage node patterns. According to the present application, although the formed photoresist pattern posses slightly enlarged corners due to underexposure, these slightly larger photoresist patterns not only compensate for losses in the amorphous layer during the subsequent etching process, but they also compensate for the reduction in size of the storage node in the subsequent rinsing process. In Lin's invention, it is necessary to utilize

the cutting mask.

From the above discussion, the Applicant believes that the amended claim 1 of the present application 5 is absolutely different from the combination of Lin's invention and Adair's invention. Reconsideration of the rejection over the amended claim 1 is hereby requested.

As claims 2 is dependent upon the amended claim 1, 10 it should be allowed if the amended claim 1 is allowed. Reconsideration of the rejection over claim 2 is therefore requested.

5. Response to Arguments

15 Applicant's arguments filed 30 January 2003 have been fully considered but they are not deemed persuasive. Applicant argues that the process involves first exposure of first exposure regions, then second cutting exposure of second exposure regions without overexposure of the cut regions due 20 to double exposure. Amended claim 1 fails to particularly point out dual exposures without overlap. In fact, use of the term "cutting" introduces new matter not supported in the original specification. In fact, the use of this term "cutting" is also vague and indefinite with respect to the question of whether 25 overlapping exposures (overexposures) should reasonably be interpreted as encompassed by this claim language.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., 30 no overexposure) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not

read into the claims. See *In re Van Genus*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Response:

5 From the response to the rejection over Claims 1-2 under 35 U.S.C. 103(a)(items 3 and 4), the Applicant believes that the amended claim 1 of the present application is absolutely different from Ueno's disclosure, Adair's disclosure, and Lin's disclosure.

10 Reconsideration of the rejection over the amended claim 1 is hereby requested.

15

20

Sincerely yours,

25  Date: 8/19/2023
Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506
Merrifield, VA 22116
U.S.A.
30 e-mail: winstonhsu@naipo.com.tw